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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/422,887	10/21/1999	RICH FOGAL	95-0134.05	6099

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EXAMINER	
BROPHY, JAMIE LYNN	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/422,887	Applicant(s) FOGAL ET AL.	
	Examiner J. L. Brophy	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12, 15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This office action is in response to the response filed 3/1/02.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 13-17 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a method of stacking chips that ensures bond pad clearance, does not reasonably provide enablement for a method of stacking chips wherein the bond pads are not accessible. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. The specification teaches a method for stacking a plurality of chips while ensuring bond pad clearance so that the wire bonding step may be performed after the chips have been stacked (see present specification, paragraph [0010]). The specification does not provide enablement for a method of stacking the chips wherein the bond pads are covered by an overlying chip. In claims 13 and 17, the limitations of "at most a minimum bond pad clearance" and "less than a maximum underlying bond pad clearance" are not in commensurate scope with the specification since the limitations read on embodiments that are outside of the range of the embodiments presented in the specification. See MPEP §2164.08.

Please note that dependent claims are rejected because the claim from which they depend has been rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7-17 are rejected under 35 U.S.C. 102(b) as being anticipated by de Givry (EP 0,489,643 A1).

Re claim 7, de Givry teaches a method of stacking a plurality of die (14, 16, 26, 28) including the steps of mounting an upper die (16) on a lower die (14) and defining a minimum angular offset with said mounting, wherein said minimum angular offset allows access to a bonding site (18) on the lower die (14). See Fig. 3 and accompanying text.

Re claim 8, de Givry teaches the step of mounting the stacked plurality of die on a substrate (12). See Fig. 2.

Re claims 9-11, de Givry teaches the steps of stacking all of the dies (14, 16, 26, 28), such that corresponding portions of any two of said dies define respective axes, and wherein said axes define an offset angle, followed by bonding wire to the dies (14, 16, 26, 28). See Fig. 3 and the third paragraph of p. 7 of the disclosure of de Givry.

Re claim 12, de Givry teaches the steps of stacking the plurality of dies (14, 16, 26, 28) along an axis, establishing an orientation for each die of said plurality of dies

(14, 16, 26, 28), marginally clearing a line of sight to contact areas of any immediately underlying die with said orientation for said each die, wherein said line of sight is parallel to said axis, and clearing a line of sight to contact areas of any underlying die with said orientation for said each die (see Fig. 3 and p. 7 of translation).

Re claims 13 and 14, de Givry teaches the steps of spiraling the plurality of chips (14, 16, 26, 28) around an axis perpendicular to the plurality of chips (14, 16, 26, 28) and ensuring at most a minimum bond pad clearance to each chip of the plurality of chips (14, 16, 26, 28), wherein spiraling the plurality of chips further comprises spiraling the plurality of chips around an axis passing through each chip (Fig. 3).

Re claims 15 and 16, de Givry teaches that the step of spiraling includes spiraling the plurality of chips around an axis passing through the center of each chip and the step of ensuring bond pad clearance further comprises rotating a chip around the axis at least to the extent that a bond pad on an underlying chip is exposed (Fig. 3).

Re claim 17, de Givry teaches the steps of serially stacking all the dies (14, 16, 26, 28) and establishing a unique orientation for each die of said all dies (14, 16, 26, 28) wherein said orientation for each die defines less than a maximum underlying bond pad (18) clearance (Fig. 3 and accompanying text).

Claims 13-15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al (5,323,060).

Re claims 13 and 14, Fogal et al teach the steps of spiraling the plurality of chips (18, 28, 54) around an axis perpendicular to the plurality of chips (18, 28, 54) and

ensuring at most a minimum bond pad (26) clearance to each chip of the plurality of chips (18, 28, 54), wherein spiraling the plurality of chips further comprises spiraling the plurality of chips around an axis passing through the center of each chip.

Re claim 17, Fogal et al teach the steps of serially stacking all the dies (18, 28, 54) and establishing a unique orientation for each die of said all dies (18, 28, 54) wherein said orientation for each die defines less than a maximum underlying bond pad (26) clearance.

See Figs. 1 and 2 and accompanying text.

Response to Arguments

Applicant's arguments filed 3/1/02 have been fully considered but they are not persuasive.

The MPEP §2164.08 states that everything within the scope of the claim must be enabled. Re claims 13-17, the specification is enabling for certain embodiments within the scope of the claims, but is not enabling for everything within the scope of the claims. Specifically, as pointed out in the above 35 U.S.C. 112, first paragraph rejection, the specification is not enabling for a method of stacking the chips wherein the bond pads are covered by an overlying chip. In fact, the present invention teaches away from such an embodiment (see present specification, paragraphs [0009] and [0010]). Applicant cites *In re Vickers* (141 F.2d 522, 61 USPQ 122 (CCPA 1944)) to support the argument that the claims are supported by embodiments addressed in the specification. However, the pending 35 U.S.C. 112, first paragraph rejection is not for *lack* of

enablement. The pending 35 U.S.C. 112, first paragraph rejection is for *scope* of enablement. The difference between the present circumstances and those in the Vickers case is that, in the Vickers case, everything within the scope of the claims was supported by the specification even though a specific embodiment was not taught by the specification. In the present case, claims 13-17 cover some embodiments which are specifically taught away from in the present specification.

Using the equations presented on p. 6 of the present specification, the following relationship exists between the minimum angle offset, α, and the maximum number of chips, N:

$$\alpha = 180 \div N$$

In Fig. 3 of the de Givry reference, there are 4 chips in the stack with an angular offset of about 45°. Using the above relationship between the number chips and the minimum angle offset, the minimum angular offset, as defined in the present specification, for 4 chips would be α=45°. Therefore, de Givry teaches a chip stack having the minimum angle offset, as defined by the present specification.

Re claim 12, in light of specification, the line of sight to contact areas is "marginally" cleared by stacking the chips with the minimum offset angle. Stacking the chips wit the minimum offset angle is taught by de Givry, as discussed in the previous paragraph.

The de Givry reference teaches that the chips 14, 16, 26 and 28 and the supports 20, 30, 32 are assembled and then cabling is carried out (see Fig. 3 and p. 7, third paragraph). Such a method anticipates claims 9-11. Applicant argues that the

Examiner previously admitted that de Givry does not teach that the bonding step is performed after all the die have been stacked. However, this previous statement made by the examiner was with regard to the embodiment taught by Fig. 1, wherein the disclosure of de Givry did not *specifically* teach that the bonding step is performed after all the die have been stacked. With regard to the embodiment of Fig. 3, the de Givry reference specifically teaches that the wiring is carried out after all of the chips and the supports have been stacked. Applicant also argues that "de Givry generally warns that stacking all of a module's chips before any wiring takes place is unworkable because the machines used to perform the wiring are capable of accommodating only a limited difference in elevation between the ends of a wire". This argument is not persuasive because the portion of the de Givry disclosure that applicant points to is referring to the embodiment of Fig. 2 wherein the 4 chips are stacked at right angles to each other. Whereas, with the embodiment of Fig. 3, de Givry teaches that the wiring can be carried out after the chips are stacked.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. L. Brophy whose telephone number is (703) 308-6182. The examiner can normally be reached on M-F (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703)

305-3432 for regular communications and (703) 308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

J.L.B.

jlb
June 18, 2002

Carl Whitehead Jr.
CARL WHITEHEAD, JR.
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